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EXAMINER	
HENDERSON, ADAM	
ART UNIT	**PAPER NUMBER**
2615	

DATE MAILED: 02/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/046,402	MABUCHI ET AL.	
	Examiner	Art Unit	
	Adam L. Henderson	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18 and 20-24* is/are rejected.

7)☒ Claim(s) *19 and 25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 January 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 3, 14, and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Kon et al. (US Patent 4,688,098).

3. With regard to claim 1 Kon et al. discloses a solid-state image pickup device (solid state image sensor, column 3 line 34 – column 8 line 11) including pixels (column 3 line 54 – column 4 line 13, FIG. 1) each of which comprises a photodiode (diodes 3, FIG. 1), a detection portion (CCD 2, FIG. 1, column 5 line 44 – column 6 line 13) and a transfer transistor (transistor 44, FIG. 4) for transferring electrons accumulated in the photodiode to the detection portion, wherein the gate voltage of said transfer transistor when the electrons are accumulated in said photodiode is set to a negative voltage (column 5 line 44 – column6 line 40) [column 6 lines 20-24 state that the voltage V_s is decreased in accordance with light intensity, thus collecting of electrons during the accumulation period; further it is not until that voltage drops to the level of the voltage V_{cd}

which is the voltage at gate (electrode 12), thus the gate must be at a negative voltage for the voltage V_s to drop to a matching voltage].

4. With regard to claim 3 Kon et al. discloses the solid-state image pickup device as claimed in claim 1, wherein the negative voltage is set to -0.5V or less (column 4 lines 41-45) [a –1 V voltage is disclosed as being applied to the gate (electrode 12)].

5. Claims 1 and 14 and claims 3 and 16 recite the same essential limitations and therefore any rejection of the device of claims 1 and 3 would inherently reject the method disclosed in claims 14 and 16.

6. Claims 4 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Tsang et al. (US Patent 5,900,623).

In regards to claims 4 and 20, both of which recite the same essential limitations, Tsang et al. describes a solid-state image pickup device (FIG. 4) including pixels (photocell 200, FIG. 4) each of which comprises a photodiode (photodiode PD, FIG. 4), a detection portion (MCAP, FIG. 4) and a transfer transistor (transistor N2, FIG. 4) for transferring holes accumulated in the photodiode to the detection portion (column 9 lines 54-65), wherein the gate voltage of said transfer transistor when the holes are accumulated in said photodiode is set to a positive voltage (column 6 line 61 – column 7 line 67) [column 7 lines 4-15 disclose that the input voltages are positive and that ground is the most negative potential on the circuit, thus the gate of the transistor must be set to a positive voltage since the most negative voltage supplied is a ground or zero voltage point; further the diode is set in a reverse-bias mode (column 5 lines 21-32), thus as dark current is created through the diode, generating a positive charge or holes].

7. Claim 10 is rejected under 35 U.S.C. 102(e) as being anticipated by Uya et al. (US Patent 6,784,935).

Uya et al. discloses a solid-state image pickup device (solid state image pickup device 3, FIG. 4) including pixels each of which comprises a photodiode (photodiodes 31, FIG. 4), a detection portion (capacitor C1, FIG. 18B) and a transfer transistor (read gate MOS transistor TR1, FIG. 18B) for transferring charges accumulated in said photodiode to said detection portion (column 10 lines 28-37), wherein an overflow path for discharging charges overflowing from said photodiode is formed in a bulk out of a channel portion of said transfer transistor and discharges the charges in a depth direction of a substrate (column 6 lines 30-43) [the overflow is referred to as a vertical overflow drain, if it overflows vertically, then it is overflowing in a depth direction as opposed to a horizontal drain which would overflow in a width or length direction].

Claim Rejections - 35 USC § 103

8. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

9. Claims 2 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kon et al. (US Patent 4,688,098) in view of Merrill (US Patent 5,892,253).

Kon et al. discloses a solid-state image pickup device as related to claims 1 and 14 above. However, there is no disclosure concerning a channel portion where the voltage is inverted. Merrill discloses the voltage under the transfer gate as being inverted (see column 2 lines 5-16).

It would have been obvious at the time of the invention to one of ordinary skill in the art to modify Kon et al. to include the voltage inverted substrate in order to allow "flow through the inverted surface region under the gate" (Merrill, column 2 lines 12-13).

10. Claims 5 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsang et al. (US Patent 5,900,623) in view of Merrill (US Patent 5,892,253).

Tsang et al. discloses a solid-state image pickup device as related to claims 4 and 20 above. However, there is no disclosure concerning a channel portion where the voltage is inverted. Merrill discloses the voltage under the transfer gate as being inverted (see column 2 lines 5-16). It would have been obvious at the time of the invention to one of ordinary skill in the art to modify Tsang et al. to include the voltage inverted substrate in order to allow "flow through the inverted surface region under the gate" (Merrill, column 2 lines 12-13).

11. Claims 6 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsang et al. (US Patent 5,900,623) in view of U.S. Patent No. 4,733,286 to Matsumoto.

Tsang et al. describes the solid-state image pickup device as claimed in claim 4 and the solid-state image pickup device driving method as claimed in claim 20, but does not teach the device wherein a positive voltage is set to a power source voltage or more. Matsumoto describes a forward voltage bias applied to a gate electrode (figure 1, item 6) and (column 2, lines 2-6). Therefore, it would have been obvious to one of ordinary skill in the art to modify the solid-state image pickup device of Tsang et al. to include a positive voltage on the gate that is set to a power source voltage or more. One would have been motivated to combine the positive voltage applied

to the photogate (PD) (Tsang et al: FIG. 4) to include the forward voltage bias (or source voltage) being applied to the gate electrode of Matsumoto in that an output which is amplified with respect to the light output (photodiode) can now be obtained (Matsumoto: column 2, lines 6-8).

12. Claims 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsang et al. (US Patent 5,900,623) in view of Nakagawa (US Patent 5,862,253).

13. With regard to claim 7, Tsang et al. claims a solid-state pickup device as described in relation to claim 4 but does not teach the device wherein an overflow path is formed of an area extended from the portion just below said photodiode to a semiconductor substrate and said area is formed of an n-type semiconductor region having an impurity concentration lower than that of a semiconductor well region or a p-type semiconductor region. Nakagawa describes semiconductor substrate formed of an n-type semiconductor region (or n-type active layer) (Nakagawa: figure 28, item 303) having an impurity concentration lower than that of a semiconductor well region (or a p-type base Layer) (Nakagawa: figure 28, item 305) (Nakagawa: column 14, lines 15-25) and (Nakagawa: column 17, claim 1). Nakagawa further describes this n-type semiconductor region (n-type active Layer 303) as a place where charges (current) are permitted to flow (overflow) (Nakagawa: column 14, lines 26-30). Particularly, Nakagawa does not describe this n-type active layer 303 as being formed in the area extended from the portion just below said photodiode to a semiconductor substrate. However, Nakagawa describes the n-type semiconductor region (or n-type buried layer 54) which is formed of a portion below the photodiode (PD) (Nakagawa: figure 13A, item PD and column 8, lines 56-65) reaching to

semiconductor substrate (or p-type semiconductor substrate 51) (Nakagawa: figure 13A, item 51) which also follows the embodiment of charge flow, which is similar to that of n-type layer 303. Therefore, it would have been obvious to one of ordinary skill in the art to modify the solid-state image pickup device of Tsang et al. to include the n-type semiconductor region impurity concentration being lower than the p-type semiconductor region and said region extending from just below the photodiode to the p-type semiconductor substrate. One would have been motivated to combine the solid-state image pickup device of Tsang et al. to include the n-type region impurity concentration lower than the p-type region and n-type region extending from below the photodiode to the p-type substrate of Nakagawa in that this embodiment would make it possible to realize a low on-state voltage even when a large current is caused to flow (Nakagawa: column 14, Lines 26-31).

14. With regard to claim 8, Tsang et al. claims a solid-state pickup device as described in relation to claim 4 but does not teach the device wherein said overflow path is formed in the area between said photodiode and said detection portion in each pixel is formed of an n-type semiconductor region having an impurity concentration Lower than that of a semiconductor well region or a p-type semiconductor region. Nakagawa describes semiconductor substrate formed of an n-type semiconductor region (or n-type active layer) (Nakagawa: figure 28, item 303) having an impurity concentration Lower than that of a semiconductor well region (or a p-type base Layer) (Nakagawa: figure 28, item 305) (Nakagawa: column 14, lines 15- 25) and (Nakagawa: column 17, claim 1). Nakagawa further describes the n-type semiconductor region (or n-type buried Layer 54), which is formed of a portion below the photodiode (PD) (Nakagawa: figure 13A, item PD and column 8, Lines 56-65) reaching to semiconductor substrate (or p-type

semiconductor substrate 51) (Nakagawa: figure 13A, item 51). Note that a photocoupler is integrally formed with the p-type semiconductor substrate 51 and functions as a current detection means of the current path, therefore comprising that of a detection portion. Since, the p- type semiconductor substrate 51 comprises that of a detection portion, then the n-type buried layer 54 does in fact fall between the area between said photodiode and the detection portion. Therefore, it would have been obvious to one of ordinary skill in the art to modify the solid-state image pickup device of Tsang et al. to include the n-type semiconductor region impurity concentration being lower than the p-type semiconductor region and said overflow path is formed in the area between said photodiode: and said detection portion. One would have been motivated to combine the solid-state image pickup device of Tsang et al. to include the n-type region impurity concentration lower than the p-type region and n-type region being in the area between the photodiode to the p-type substrate of Nakagawa in that this embodiment would make it possible to realize a low on-state voltage even when a large current is caused to flow (Nakagawa: column 14, Lines 26-31).

15. With regard to claim 9, Tsang et al. claims a solid-state pickup device as described in relation to claim 4 but does not teach the device wherein an overflow path is formed of an area extending from the portion just below said photodiode and the area between said photodiode and said detection portion to a semiconductor substrate in each pixel is formed of an n-type semiconductor region having an impurity concentration lower than that of a semiconductor well region or a p-type semiconductor region. Nakagawa describes semiconductor substrate formed of an n-type semiconductor region (or n-type active layer) (Nakagawa: figure 28, item 303) having an impurity concentration lower than that of a semiconductor well region (or a p-type base layer)

(Nakagawa: figure 28, item 305) (Nakagawa: column 14, Lines 15-25) and (Nakagawa: column 17, claim 1). Nakagawa further describes this n-type semiconductor region (n-type active Layer 303) as a place where charges (current) are permitted to flow (overflow) (Nakagawa: column 14, Lines 26-30). Particularly, Nakagawa does not describe this n-type active layer 303 as being formed in the area extended from the portion just below said photodiode to a semiconductor substrate. However Nakagawa describes the n-type semiconductor region (or n-type buried Layer 54) which is formed of a portion below the photodiode (PD) (Nakagawa: figure 13A, item PD and column 8, lines 56-65) reaching to semiconductor substrate (or p-type semiconductor substrate 51) (Nakagawa: figure 13A, item 51) which also follows the embodiment of charge flow, which is similar to that of n-type Layer 303. Keep in mind that this area described as "below the photodiode" simultaneously comprises that of the "area between said photodiode and said detection portion," since the p-type semiconductor substrate 51 comprises that of a detection portion, then the n-type buried layer 54 does in fact fall between the area between said photodiode and the detection portion. Therefore, it would have been obvious to one of ordinary skill in the art to modify the solid-state image pickup device of Tsang et al. to include the n-type semiconductor region impurity concentration being lower than the p-type semiconductor region and overflow path is formed of an area extending from the portion just below said photodiode and the area between said photodiode and said detection portion to a semiconductor substrate. One would have been motivated to combine the solid-state image pickup device of Tsang et al. to include the n-type region impurity concentration lower than the p-type region and n-type region extending from below the photodiode to the p-type substrate of Nakagawa in that this

embodiment would make it possible to realize a Low on-state voltage even when a large current is caused to flow (Nakagawa: column 14, lines 26-31).

16. Claims 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Uya et al. (US Patent 6,784,935) in view of Nakagawa (US Patent 5,862,253).

17. With regard to claim 11, Uya et al. discloses a solid-state image pickup device as related to claim 10, but does not teach the device wherein an overflow path is formed of an area extended from the portion just below said photodiode to a semiconductor substrate and said area is formed of an n-type semiconductor region having an impurity concentration lower than that of a semiconductor well region or a p-type semiconductor region. Nakagawa describes semiconductor substrate formed of an n-type semiconductor region (or n-type active layer) (Nakagawa: figure 28, item 303) having an impurity concentration Lower than that of a semiconductor well region (or a p-type base Layer) (Nakagawa: figure 28, item 305) (Nakagawa: column 14, lines 15-25) and (Nakagawa: column 17, claim 1). Nakagawa further describes this n-type semiconductor region (n-type active Layer 303) as a place where charges (current) are permitted to flow (overflow) (Nakagawa: column 14, lines 26-30). Particularly, Nakagawa does not describe this n-type active layer 303 as being formed in the area extended from the portion just below said photodiode to a semiconductor substrate. However, Nakagawa describes the n-type semiconductor region (or n-type buried layer 54) which is formed of a portion below the photodiode (PD) (Nakagawa: figure 13A, item PD and column 8, lines 56-65) reaching to semiconductor substrate (or p-type semiconductor substrate 51) (Nakagawa: figure 13A, item 51) which also follows the embodiment of charge flow, which is similar to that of n-type layer 303.

Therefore, it would have been obvious to one of ordinary skill in the art to modify the solid-state image pickup device of Uya et al. to include the n-type semiconductor region impurity concentration being lower than the p-type semiconductor region and said region extending from just below the photodiode to the p-type semiconductor substrate. One would have been motivated to combine the solid-state image pickup device of Uya et al. to include the n-type region impurity concentration lower than the p-type region and n-type region extending from below the photodiode to the p-type substrate of Nakagawa in that this embodiment would make it possible to realize a low on-state voltage even when a large current is caused to flow (Nakagawa: column 14, Lines 26-31).

18. With regard to claim 12, Uya et al. discloses a solid-state image pickup device as related to claim 10, but does not teach the device wherein said overflow path is formed in the area between said photodiode and said detection portion in each pixel is formed of an n-type semiconductor region having an impurity concentration lower than that of a semiconductor well region or a p-type semiconductor region. Nakagawa describes semiconductor substrate formed of an n-type semiconductor region (or n-type active layer) (Nakagawa: figure 28, item 303) having an impurity concentration lower than that of a semiconductor well region (or a p-type base Layer) (Nakagawa: figure 28, item 305) (Nakagawa: column 14, lines 15- 25) and (Nakagawa: column 17, claim 1). Nakagawa further describes the n-type semiconductor region (or n-type buried Layer 54), which is formed of a portion below the photodiode (PD) (Nakagawa: figure 13A, item PD and column 8, Lines 56-65) reaching to semiconductor substrate (or p-type semiconductor substrate 51) (Nakagawa: figure 13A, item 51). Note that a photocoupler is integrally formed with the p-type semiconductor substrate 51 and functions as a current detection

means of the current path, therefore comprising that of a detection portion. Since, the p- type semiconductor substrate 51 comprises that of a detection portion, then the n-type buried layer 54 does in fact fall between the area between said photodiode and the detection portion. Therefore, it would have been obvious to one of ordinary skill in the art to modify the solid-state image pickup device of Uya et al. to include the n-type semiconductor region impurity concentration being lower than the p-type semiconductor region and said overflow path is formed in the area between said photodiode: and said detection portion. One would have been motivated to combine the solid-state image pickup device of Uya et al. to include the n-type region impurity concentration lower than the p-type region and n-type region being in the area between the photodiode to the p-type substrate of Nakagawa in that this embodiment would make it possible to realize a low on-state voltage even when a large current is caused to flow (Nakagawa: column 14, Lines 26-31).

19. With regard to claim 13, Uya et al. discloses a solid-state image pickup device as related to claim 10, but does not teach the device wherein an overflow path is formed of an area extending from the portion just below said photodiode and the area between said photodiode and said detection portion to a semiconductor substrate in each pixel is formed of an n-type semiconductor region having an impurity concentration lower than that of a semiconductor well region or a p-type semiconductor region. Nakagawa describes semiconductor substrate formed of an n-type semiconductor region (or n-type active layer) (Nakagawa: figure 28, item 303) having an impurity concentration lower than that of a semiconductor well region (or a p-type base layer) (Nakagawa: figure 28, item 305) (Nakagawa: column 14, lines 15-25) and (Nakagawa: column 17, claim 1). Nakagawa further describes this n-type semiconductor region (n-type active Layer

303) as a place where charges (current) are permitted to flow (overflow) (Nakagawa: column 14, Lines 26-30). Particularly, Nakagawa does not describe this n-type active layer 303 as being formed in the area extended from the portion just below said photodiode to a semiconductor substrate. However Nakagawa describes the n-type semiconductor region (or n-type buried Layer 54) which is formed of a portion below the photodiode (PD) (Nakagawa: figure 13A, item PD and column 8, lines 56-65) reaching to semiconductor substrate (or p-type semiconductor substrate 51) (Nakagawa: figure 13A, item 51) which also follows the embodiment of charge flow, which is similar to that of n-type layer 303. Keep in mind that this area described as "below the photodiode" simultaneously comprises that of the "area between said photodiode and said detection portion," since the p-type semiconductor substrate 51 comprises that of a detection portion, then the n-type buried layer 54 does in fact fall between the area between said photodiode and the detection portion. Therefore, it would have been obvious to one of ordinary skill in the art to modify the solid-state image pickup device of Uya et al. to include the n-type semiconductor region impurity concentration being lower than the p-type semiconductor region and overflow path is formed of an area extending from the portion just below said photodiode and the area between said photodiode and said detection portion to a semiconductor substrate. One would have been motivated to combine the solid-state image pickup device of Uya et al. to include the n-type region impurity concentration lower than the p-type region and n-type region extending from below the photodiode to the p-type substrate of Nakagawa in that this embodiment would make it possible to realize a low on-state voltage even when a large current is caused to flow (Nakagawa: column 14, Lines 26-31).

20. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kon et al. (US Patent 4,688,098) in view of Isogai et al. (US Patent 5,942,774).

Kon et al. discloses a solid-state image pickup device as related to claim 14 but does not disclose that electrons overflow to the substrate. Isogai et al. disclose in column 16 lines 66-67 the use of the substrate as a location to send overflow. It would have been obvious at the time of the invention to one of ordinary skill in the art to modify the solid-state image pickup device of Kon et al. to include the transmission of overflow to the substrate as taught by Isogai et al. in order to suppress blooming and smear (column 8 lines 60-63).

21. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kon et al. (US Patent 4,688,098) in view of Suzuki (US Patent 6,002,123).

Kon et al. discloses a solid-state image pickup device as related to claim 14 but does not disclose that electronsoverflow to the channel of a transistor. Suzuki discloses the excess charge overflowing into the channel of a transistor (column 8 lines 18-21). It would have been obvious at the time of the invention to one of ordinary skill in the art to modify Kon et al. to include the overflow into the channel of a transistor as taught by Suzuki in order to prevent blooming (column 8 lines 28-38).

22. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsang et al. (US Patent 5,900,623) in view of Isogai et al. (US Patent 5,942,774).

Tsang et al. discloses a solid-state image pickup device as related to claim 20 but does not disclose that holes overflow to the substrate. Isogai et al. disclose in column 16 lines 66-67

the use of the substrate as a location to send overflow. It would have been obvious at the time of the invention to one of ordinary skill in the art to modify the solid-state image pickup device of Tsang et al. to include the transmission of overflow to the substrate as taught by Isogai et al. in order to suppress blooming and smear (column 8 lines 60-63).

23. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsang et al. (US Patent 5,900,623) in view of Suzuki (US Patent 6,002,123).

Tsang et al. discloses a solid-state image pickup device as related to claim 20 but does not disclose that holes overflow to the channel of a transistor. Suzuki discloses the excess charge overflowing into the channel of a transistor (column 8 lines 18-21). It would have been obvious at the time of the invention to one of ordinary skill in the art to modify Tsang et al. to include the overflow into the channel of a transistor as taught by Suzuki in order to prevent blooming (column 8 lines 28-38).

Allowable Subject Matter

24. Claims 19 and 25 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

25. Applicant's arguments with respect to claims 1-18 and 20-24 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

26. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Adam L. Henderson whose telephone number is 571-272-8619. The examiner can normally be reached on Monday-Friday, 6am to 2:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ngoc-Yen Vu can be reached on 571-272-7320. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ALH
16 February 2006

NGOC-YEN VU
PRIMARY EXAMINER